High-Speed Link Tuning Using Signal Conditioning Circuitry in Stratix V Transceivers

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This application note provides a set of guidelines to run error free across backplanes at high-speed data rates by tuning the analog settings available in Stratix® V transceivers. Various high-speed protocols target certain bit error ratio (BER) requirements. Meeting a BER of $1E^{-12}$ or lower over lossy backplanes and connectors can be very challenging. Stratix V transceivers are equipped with link tuning capabilities that will help you meet the stringent BER requirements.

This application note contains three sections: an introductory section describing the link tuning capabilities and loss compensation profile, and two typical case studies enumerating the steps involved in tuning a backplane link.

Note: Altera recommends that you understand the link tuning capabilities covered in the "Backplane Applications with 28 nm FPGAs" White Paper before using this application note.

Related Information

Backplane Applications with 28 nm FPGAs White Paper

Backplane Link Tuning Methodology

Backplane systems introduce insertion loss, reflections, and crosstalk to channel data, which degrade the signal's integrity. All of the above losses reduce the eye opening at the receiver (RX). The non-uniform loss over frequencies also causes inter-symbol interference (ISI).

Stratix V transceivers are designed with link tuning features to handle channel degradation for data rates up to 12.5 Gbps. The link tuning features are as follows:

- Programmable transmitter (TX) voltage output differential (VOD) and pre-emphasis
- Continuous time linear equalizer (CTLE) or adaptive equalizer (AEQ)
- Decision feedback equalizer (DFE)

Table 1: Link Tuning Features and Typical Insertion Loss Capability

Feature	Typical Loss Compensation at Nyquist (dB)
TX pre-emphasis	Up to 12
CTLE	Up to 16
CTLE with DFE	Over 22
CTLE, DFE, and TX pre-emphasis	Over 25

The TX VOD, TX pre-emphasis (1st post-tap, pre-tap, and 2nd post-tap), RX equalization and DFE are controlled using the transceiver reconfiguration controller. Select **Enable Analog controls** in the transceiver reconfiguration controller to enable the TX VOD and pre-emphasis settings. Select the **Enable decision feedback equalizer (DFE)** and **Enable adaptive equalization (AEQ)** options in the transceiver reconfiguration controller to enable the DFE and AEQ blocks, respectively.

The transceiver reconfiguration controller provides an Avalon® memory mapped user interface to step through the various analog parameter settings. You can choose to create your own user logic in the FPGA fabric to control the reconfiguration controller, or use a transceiver toolkit design.

Note: Refer to the "Altera Transceiver PHY IP User Guide" for reconfiguration controller implementation and steps to control these analog settings.

Related Information

Altera Transceiver PHY IP Core User Guide

Case Studies

The case studies in the following sections describe the block diagram of the designs used for link tuning, steps to tune the backplane link, and the observed results.

- Tuning a **Medium reach backplane** (24” backplane) with insertion loss of ~19.5 dB and low return loss. The BER requirements of this backplane can be met using CTLE and TX pre-emphasis.
- Tuning a **10GBASE-KR compliant backplane** (30" backplane) with insertion loss of ~25 dB. The BER requirements of this backplane can be met by using the TX pre-emphasis, CTLE, and DFE.

Note: Use the associated reference design for **High-Speed Link Tuning** to evaluate and implement the link tuning design. The "High-Speed Link Tuning Reference Design User Guide" in the zip folder provides step-by-step procedures to use the reference design.

Related Information

High-Speed Link Tuning

Tuning a Medium Reach Backplane with Insertion Loss of ~19.5 dB

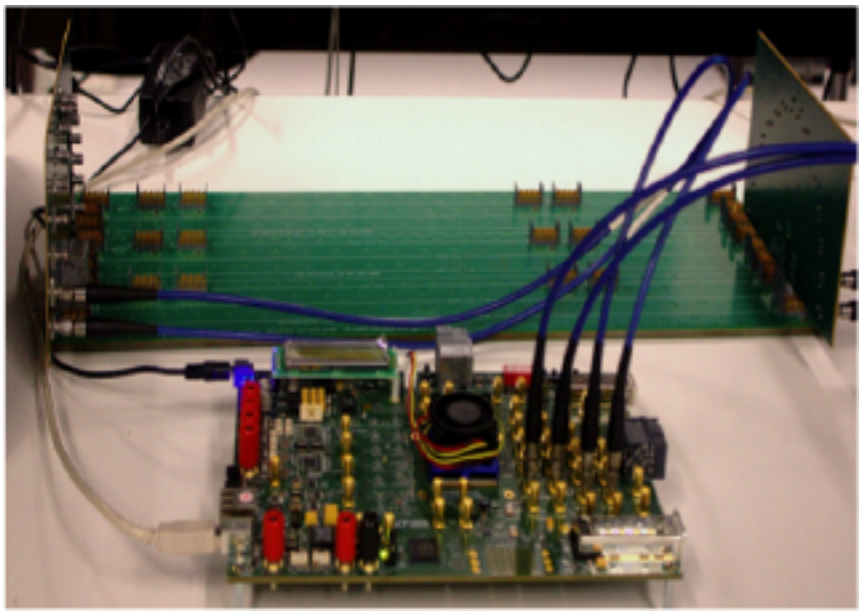
This case study explains the steps to tune a 24” backplane running at 10.3 Gbps with an insertion loss of ~19.5 dB. An insertion loss of 16 dB is contributed by the backplane itself, and 4 dB is contributed by the cables and Stratix V Signal Integrity (SI) evaluation board.

Transceiver Link Setup

To set up the transceiver link:

1. Connect the serial data output from channel 0’s TX to one end of the backplane.
2. Connect the other end of the backplane to the serial data input of channel 0’s RX.

Figure 1: Stratix V SI Board and Amphenol Backplane Lab Setup

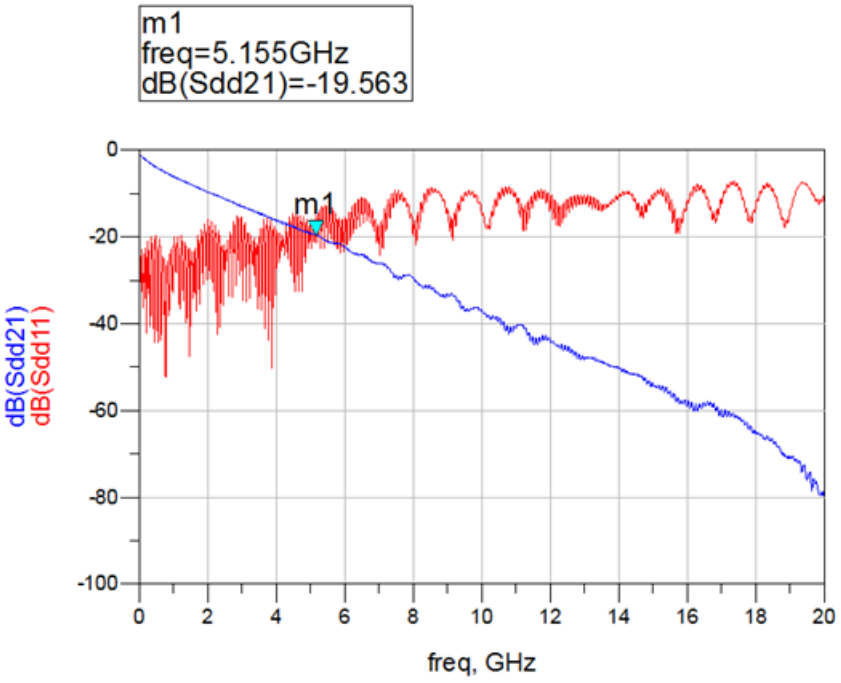


Backplane Specifications

The backplane used for this case study is a 24” Amphenol Nelco (N4K12SI) backplane. It has an Xcede daughter card connected at each end of the backplane.

Figure 2: Insertion Loss of 24" Amphenol Backplane with Stratix V 10.3 Gbps Link

Based on the VNA measurements for the system setup shown in the previous figure, the insertion loss is ~19.5 dB at the Nyquist frequency of 5.15625 GHz.

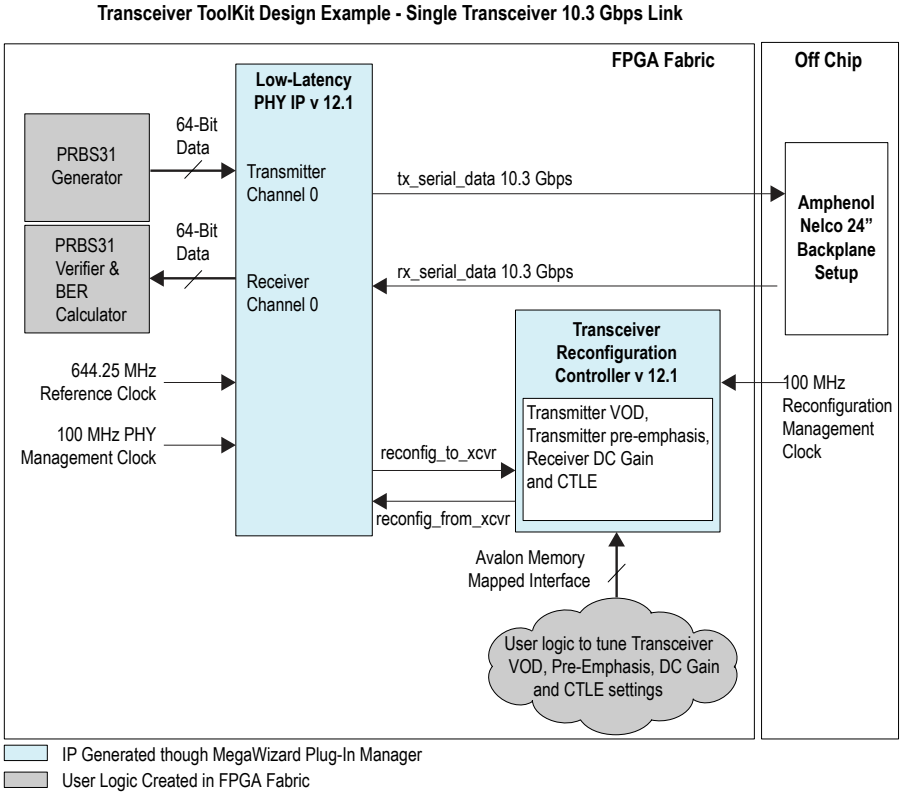


Implementing the Transceiver Design

This case study uses the transceiver toolkit to tune the TX and RX settings for a given backplane. The design was implemented using the Quartus® II software version 12.1, and serves as a reference for similar backplanes.

Figure 3: Block Diagram of Reference Design for Case Study 1

You can choose to use this reference design along with a Stratix V SI board to tune your backplane or create your own design with the blocks described in the following figure.

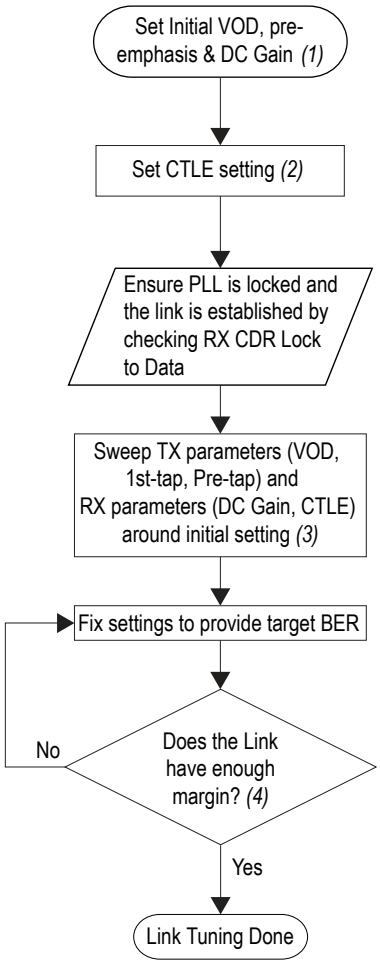


Transceiver Link Tuning Flow

Altera recommends the steps shown in the following flowchart to achieve 0 BER for transceiver links similar to the one shown in this case study.

Figure 4: Recommended Flow for Transceiver Link Tuning

The numbers in parentheses refer to the notes following the figure.



Notes

1. You can set the initial values for the TX VOD, TX pre-emphasis, and RX DC gain in two ways:
   - Simulation approach using pre-emphasis and the equalization link estimator (PELE).

     Note: For more information on the PELE approach to link tuning, refer to the Stratix V FPGA Signal and Power Integrity Center.

- Analytical approach by understanding the following link requirements:
  - The Stratix V RX requires a peak-to-peak input voltage amplitude of 400 mV for adaptive equalization. The VOD must have enough swing to compensate for backplane losses at lower frequencies and be able to provide 400 mv peak-to-peak at the RX input. The typical backplane low frequency loss is ~3 dB. Therefore, the transmitter VOD must be greater than ~550 mV. For this case study, an initial VOD setting of 50 is selected.
  - Pre-tap and post-tap compensate for pre-cursor and post-cursor ISI: A negative pre-tap and first post-tap improve the high frequency content additively. You can choose initial values in the middle range for both 1st post-tap and negative pre-tap. For this case study, the initial value chosen for the 1st post-tap was 15 and pre-tap was -7.
  - DC gain improves the eye envelope. Altera recommends an initial value of 3 dB DC gain (setting 1).

2. To set CTLE, you can use AEQ one-time to automatically compute the initial CTLE value or choose a value that compensates for the insertion loss of the backplane without over equalizing the signal. For this case study, the insertion loss is 19.5 dB at the Nyquist frequency. Therefore, a CTLE setting of 15 was chosen as the initial value because it provides the maximum compensation for insertion loss.
3. To sweep the analog parameters, use the transceiver reconfiguration controller. The transceiver reconfiguration controller does not check for legal combinations of the TX analog parameters. Use the **Stratix V Legal PMA Setting Check** tool to determine the legal TX PMA settings.
4. Estimate the transceiver link margin in the following ways:
   a. Use EyeQ to measure the horizontal and vertical opening of the eye at the CDR input. Choose the setting that provides the best eye opening.
   b. Find the middle value amongst the possible solution spaces for each setting so that the variation of these settings across PVT (process, voltage, temperature) is accounted for. In this case study, the TX or RX parameter range of values that provides the target BER is called the **solution space**.
   c. Increase the BER testing target (e.g. from 10^{-12} to 10^{-15}) and find solutions that meet this new target BER. Testing for a higher BER target increases the link margin. This case study uses a combination of methods (b) and (c) for link margin evaluation.

Related Information

- **Stratix V FPGA Signal and Power Integrity**
- **Stratix V Legal PMA Setting Check**

Results

All the results have been captured for the transceiver channel 0 of the reference design and the Xcede differential pair.

It is possible to arrive at various combinations of analog parameters that give you a 0 BER. You can follow the methods explained in steps **3** and **4** above to choose the final solution for your link.

Note: A comprehensive list of results (Tuning_Medium_reach_Backplane_Insertion_Loss_20dB_Stratix V_Results.xlsx) is available in the "High Speed Link Tuning" reference design.

Table 2: PMA Settings for BER of 1 x 10^{-12} for ~19.5 dB Loss Medium Reach Backplane

The following table shows the results chosen for this case study.

VOD = 59, Pre-emphasis 1st Post-tap = 13, Pre-emphasis Pre-tap = -13				
PRBS31	dc=0	dc=1	dc=2	dc=3
CTLE Setting = 12	0	2.35E-08	4.07E-05	0.003293
CTLE Setting = 13	0	1.16E-09	9.54E-06	0.001424
CTLE Setting = 14	0	0	5.29E-07	1.35E-04
CTLE Setting = 15	2.08E-10	0	1.52E-08	9.56E-06

Table 3: Final Solution for ~19.5 dB Loss Medium Reach Backplane Tuning

Backplane	24" Amphenol
Backplane + Board loss @ 5.156	19.5 dB
TX VOD	59
TX 1st Post-tap	13
TX Pre-tap	-13
TX 2nd Post-tap	0
CTLE Setting	14
DC Gain Setting	0
BER with CTLE	0

Related Information

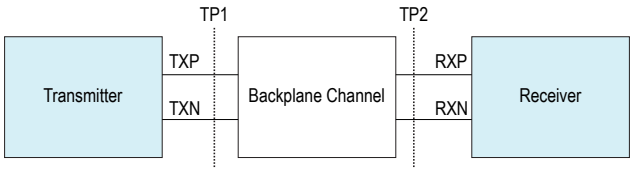
High-Speed Link Tuning

Tuning a 10GBASE-KR Compliant Backplane

For this case study, a 30" FCI backplane with paddle cards on both ends was used as the backplane channel. Backplane ethernet standards use informative parameters (insertion loss, return loss, and insertion loss to crosstalk ratio) to evaluate the backplane channel.

Figure 5: Typical Backplane Channel with Transceiver

The backplane interconnect is defined between TP1 and TP2, as shown in the figure below.



For 10GBASE-KR, the maximum insertion loss (ILmax) between TP1 and TP2 at the Nyquist frequency of 5.15625 GHz is 25.2 dB.

Figure 6: Stratix V SI Board and FCI Backplane Lab Setup

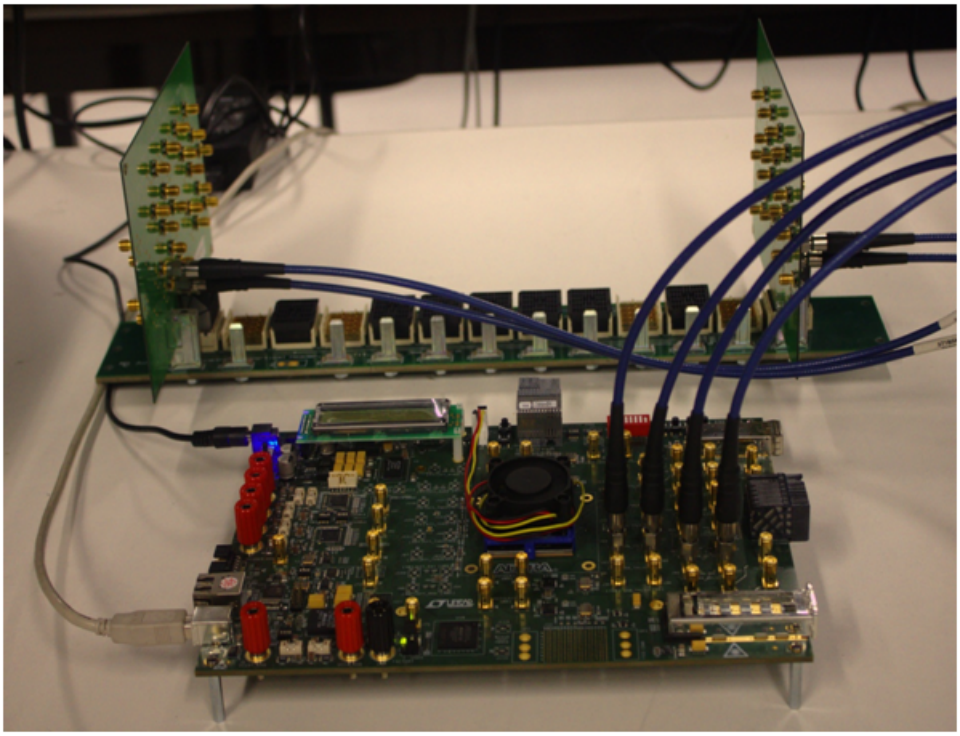
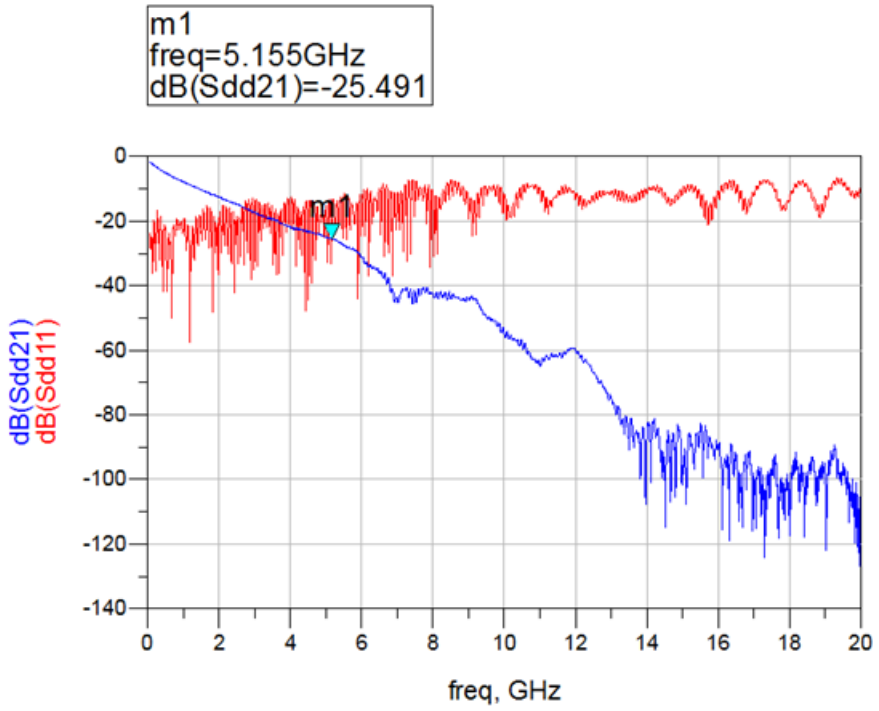


Figure 7: Insertion and Return Loss Characteristics of 30" FCI Backplane Channel

The insertion loss of the backplane channel (TX to 30" FCI backplane to RX) from VNA measurements is 25.49 dB, as shown in the following figure. The backplane channel is within the high confidence region defined by 10GBASE-KR and is compliant with the 10GBASE-KR standard.



Implementing a Transceiver Design for 10GBASE-KR Link Tuning

The three modes of operation for Stratix V DFE are Manual mode, Continuous mode, and Triggered mode. There are a total of 354,375 DFE tap combinations that can be selected in Manual mode. To minimize the time to select DFE taps, Altera recommends Continuous or Triggered Mode.

Table 4: Stratix V Link Tuning Feature Performance Guidelines

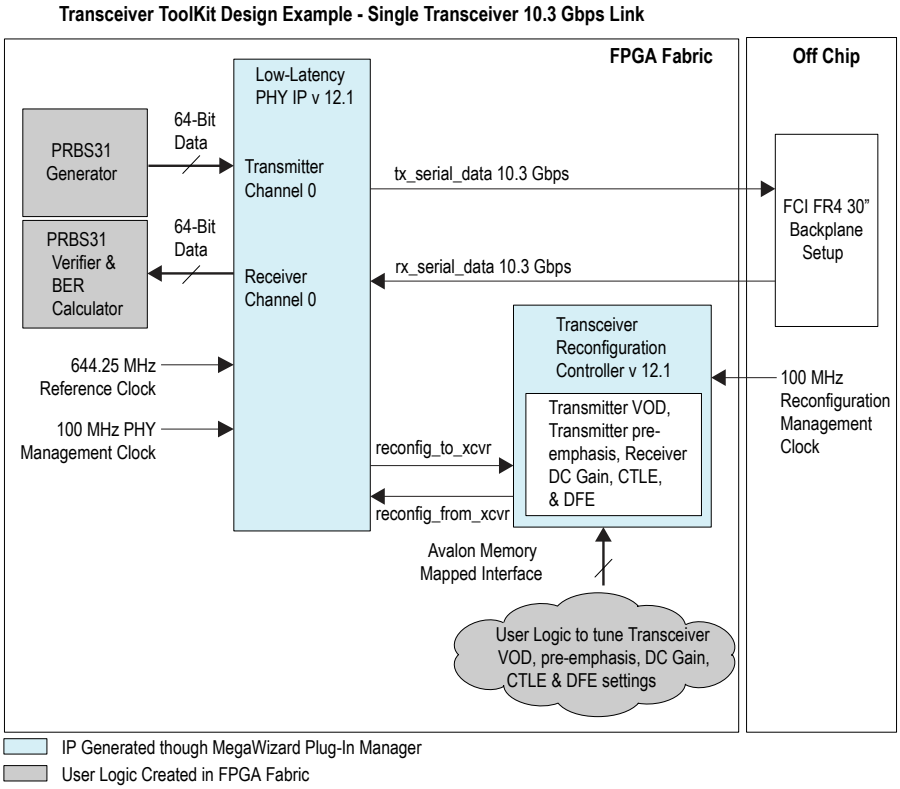
Data Rate (Gbps)	Insertion Loss (dB)	TX pre-emphasis			RX Equalization		
		VOD	1st Post-tap	Pre-tap	CTLE Setting	DC Gain Setting	DFE Mode
Up to 10.3	Up to 20	50	0	0	15	0	Triggered
	Up to 25	60	15	-15	15	1	Triggered
Up to 11.1	Up to 20	60	15	-15	15	1	Triggered
	Up to 25	60	15	-15	15	1	Triggered

Data Rate (Gbps)	Insertion Loss (dB)	TX pre-emphasis			RX Equalization		
		VOD	1st Post-tap	Pre-tap	CTLE Setting	DC Gain Setting	DFE Mode
Up to 12.5	Up to 20(1)	47	20	-15	14	1	Triggered
	Up to 25(1)	60	15	-15	14	1	Triggered

The 10GBASE-KR link loss of 25.4 dB can be compensated by using the TX pre-emphasis and CTLE, DFE Triggered mode.

Figure 8: Block Diagram of Reference Design for 10GBASE-KR Backplane Tuning

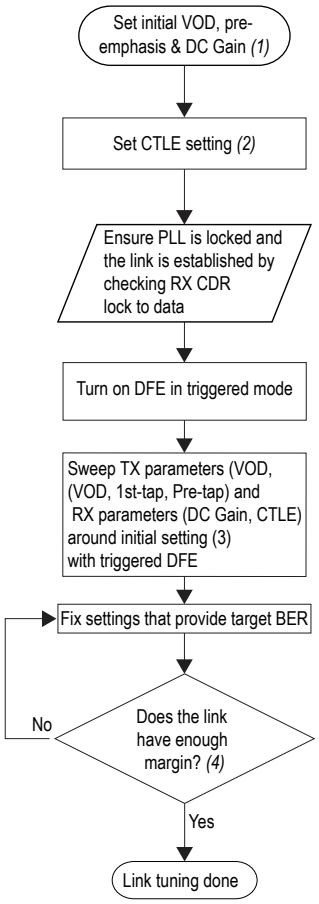
The following figure shows the block diagram of the reference design used in this link tuning. The design was implemented using Quartus II software version 12.1.



(1) These conditions require a training sequence at power-up to calibrate the link. Contact Altera for additional details.

Figure 9: Recommended Flow for 10GBASE-KR Compliant Link Tuning

The numbers in parentheses refer to the notes following the figure.



Notes

1. Refer to the Notes for the "Recommended Flow for Transceiver Link Tuning" figure.
2. To set CTLE, you can use AEQ one time to automatically compute the initial CTLE value or choose a value that compensates for the insertion loss of the backplane without over equalizing the signal. For this case study, the insertion loss is 25 dB at the Nyquist frequency. Therefore, a CTLE setting of 15 was selected as the initial value because it provides the maximum compensation for insertion loss.
3. You can sweep the analog parameters using the transceiver reconfiguration controller. The transceiver reconfiguration controller does not check for legal combinations of the TX analog parameters. Use the **Stratix V Legal PMA Setting Check** tool to determine the legal TX PMA settings. For every change in a PMA analog control, you must re-run a DFE triggered adaptation to get new DFE tap coefficients that will compensate for changes in signal conditioning.
4. The transceiver link margin can be estimated in the following ways:
   a. Use EyeQ to measure the horizontal and vertical opening of the eye at the CDR input. Choose the setting that provides the best eye opening. When DFE is used, Altera recommends that you set the

EyeQ monitor in 1D mode. Refer to the "Altera Transceiver PHY IP Core User Guide" for 1D EyeQ mode implementation details.

b. Find the middle value among the possible solution spaces for each setting so that the variation of these settings across PVT (process, voltage, temperature) is accounted for. In this case study, the TX or RX parameter range of values that provides the target BER is called the **solution space**.

c. Increase the BER testing target (e.g. from 10^{-12} to 10^{-15}) and find solutions that meet this new target BER. This case study uses a combination of (b) and (c) for link margin evaluation.

Related Information

- **Stratix V Legal PMA Setting Check**
- **Altera Transceiver PHY IP Core User Guide**

Results

All the results have been captured for the transceiver channel 0 of the reference design. A comprehensive list of results (10GBaseKR_compliant_backplane_link_tuning_StratixV_Results.xlsx) is available in the "High Speed Link Tuning" reference design.

The BER is checked for $3x10^{12}$ bits to achieve a BER of $1x10^{-12}$ with a confidence level of 95%. Based on results, considering VT tolerance and BER confidence level, the final solution for this backplane tuning is listed in the following table.

Table 5: PMA Settings Resulting in BER of $1x10^{-12}$ for 10GBASE-KR Compliant Backplane

TX Settings				RX Settings		
VOD	1st Post-tap	Pre-tap	2nd Post-tap	CTLE	DC gain	DFE
45 to 50	15 to 20	-15 to -10	0	14 to 15	1	Triggered

Table 6: Backplane 30" FCI

The following table lists the final solution for 10GBASE-KR compliant backplane tuning.

Backplane	30" FCI
Backplane + Board loss @ 5.156	25.4 dB
TX VOD	48
TX 1st Post-tap	17
TX Pre-tap	-13
TX 2nd Post-tap	0
CTLE setting	14
BER with CTLE and triggered DFE	0

Related Information

High-Speed Link Tuning

Document Revision History

Table 7: Document Revision History

Date	Version	Changes
February 2015	2015.02.26	Clarified Note 1 in the "Recommended Flow for 10GBASE-KR Compliant Link Tuning" figure.
March 2013	2013.03.19	Initial release.