Variability and reliability analysis of CNFET in the presence of manufacturing imperfections

Carmen G. Almudéver and Antonio Rubio
1. Introduction

2. CNFET manufacturing process imperfections

3. Simulation methodology of CNFET manufacturing variability

4. CNFET reliability analysis

5. CNFET variability study

6. Conclusions
Introduction: LOGIC SCALING ROADMAP

Strain engineering techniques
Advanced gate stack engineering
Fully-depleted channel electrostatics
Band-engineered channel for enhanced transport

SD stressors
High-K Metal gate
Multigate FETs
III/V & Ge channels

Stress Liner

nMOS pMOS

Bulk FinFET

Quantum well devices

Intel 1st generation High-K Metal Gate
Intel 2nd generation High-K Metal Gate

Intel Tri-Gate transistor

Tech. node

32/28nm

14nm

7nm

45nm

22/20nm

10nm

5nm

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Introduction: LOGIC SCALING ROADMAP

New transport & extreme channel electrostatics

Nanowires Tunnel FETs
Graphene FETs
Carbon Nanotube FETs

Charge based Beyond CMOS
Spin FETs, IMOS, NEMS switch, Atomic switch, MOTT FET...

Non-FET, Non-charge based Beyond CMOS
Spin Wave device, Nanomagnetic Logic, Excitonic FET, BisFET, All Spin Logic...

Tech. node

10nm
7nm
5nm

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Introduction: CARBON NANOTUBES

1D

Multi-wall CNT (Sumio Iijima, 1991)
Single-wall CNT (D.S Bethune, S. Ijima 1993)

Chirality: \[ C_h = na_1 + ma_2 \equiv (n,m) \]

- **Diameter**
  \[ D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} \]
  \[ a_0 = 0.142 \text{nm} \]

- ** Behaviour**
  Rest of \[ \left[ (n - m)/3 \right] = 0 \quad \rightarrow \quad \text{Metallic} \]
  Rest of \[ \left[ (n - m)/3 \right] \neq 0 \quad \rightarrow \quad \text{Semiconducting} \]
Introduction: CARBON NANOTUBES

Carbon Nanotube Field Effect Transistors (CNFETs) are promising candidates as a potential extension to Si-MOSFETs.

- Recent studies show that with 200 CNTs/μm, sub-10nm CNFETs can potentially outperform Si CMOS transistors, including Si FinFETs, Si nanowires and Si ETSOI FETs [Franklin 12].

- CNFETs have also been experimentally demonstrated to operate at a very low supply voltage of 0.4V [Ding 12].

- For CNFET-based digital systems, shows that “ideal” CNFET technology can be 5x faster than Si-CMOS (partially-depleted SOI) while consuming the same power at the 11nm technology node [Wei 09]
Introduction: CARBON NANOTUBES

CNFETs are also affected by manufacturing imperfections and several challenges must be overcome before such benefits can be realized.

- Presence of m-CNTs
- CNT density variations
- CNT diameter variations
- CNT alignment variations
- CNT doping variations

TOPIC & OBJECTIVE

To study the impact of today’s manufacturing imperfections on CNFET performance and reliability giving a realistic view of the current status of CNT technology.
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CNFET manufacturing imperfections

CNT doping variations and low Metal-CNT contact resistance

- Stable high-performance p-type CNFETs have been demonstrated through high work-function metal contacts
- Realization of high-performance n-type CNFETs that are stable in ambient air still remains a challenge:
  1. Low-work function metal contacts [Shahrjerdi 13]
  2. ALD-based electrostatic doping [Wei 11]
- Non-ideal wetting of metal to CNT
  1. Graphitic carbon interfacial layers [Chai 12]
- Presence of Schottky-Barrier (SB) between metal and the CNT due to band misalignment
  1. Selection of contact metal with proper work-function
CNFET manufacturing imperfections

Alignment and positioning of CNFETs

SEM image of a pattern of perfectly aligned, perfectly linear SWNTs formed by CVD growth on a quartz substrate [Kang 07]

Experimental demonstration of misaligned and mispositioned CNT-immune logic structures. SEM images of logic structures corresponding to (a) NAND, (b) NOR, (c) AND–OR–INVERT, and (d) OR–AND–INVERT pull-ups [Patil 08].
Diameter CNT variations

Chirality is responsible for the random distribution of CNT diameters.

Role of diameter variation on $V_{TH}$ variation [Ray 09]

Role of diameter variation on the means $I_{ON}$ and $I_{OFF}$ of a single CNFET channel [Ray 09]

$$E_{gap} = \frac{0.84}{d(nm)} (eV)$$

1. Improvements in CNT synthesis [Ghorannevis 12]
2. Solution Based CNT Sorting [Seo 13]
CNFET manufacturing imperfections

CNT density variations

- These variations are due to the non-uniform spacing between CNTs (non-uniform pitch) during the CNT growth resulting in variations in the number of CNTs in the transistor.
- The increase of CNT density: The average CNT density obtained today using CVD technique is between 1-10 CNTs/μm.

**multiple-growth** [Hong 10]  
**multiple-transfer** [Shulaker 11, Wang 10]

- 45 CNTs/μm
- 55 CNTs/μm

Tube density of more than **500 CNTs/μm** can be prepared from solution via methods such as Langmuir–Schaefer technique [Cao 13]
CNFET manufacturing imperfections

Presence of m-CNTs

With a typical CNT synthesis process 1/3 of CNTs are metallic and 2/3 are semiconducting.

1. Plasma Enhanced CNT Synthesis : 4%-10 % m-CNTs [Qu 08]
2. Solution Based CNT Sorting : 1%-5% m-CNTs [LeMieux 08]
3. m-CNTs removing techniques [Zhang 06][Collins 01] [Wei 10]
   (SDB, gas phase and chemical reaction, VMR )

Selective etching of metallic carbon nanotubes from the gas phase [Zhang 06]

Images of partially broken SWNTs show clear thinning. [Collins 01]

VMR is a VLSI-compatible technique using inter-digitated electrodes [Wei 10]

Thermocapillary-resist approach [Jin 13]
Relative contributions of CNT-specific variations to CNFET on-current variations

Presence of m-CNTs and CNT count variations are the main sources of CNFET failure.

- **SHORT**: Presence of 1 or more m-CNT in the CNFET
- **OPEN**: There is no CNT bridging the source and drain contacts

Relevance of CNFET manufacturing imperfections [Zhang 11]
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Simulation of CNFET manufacturing variability

HSPICE Stanford CNFET compact model

<table>
<thead>
<tr>
<th>$I_{ON}$</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$V_{TH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>47.89 μA</td>
<td>$1 \times 10^6$</td>
<td>0.29 V</td>
</tr>
</tbody>
</table>

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Simulation of CNFET manufacturing variability

We have developed a methodology of analysis based on a MATLAB script in order to analyze the variability and reliability of CNFETs due to the following imperfections:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Distribution</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT diameter variations (D)</td>
<td>Gaussian distribution</td>
<td>[Patil 09a]</td>
</tr>
<tr>
<td></td>
<td>$\mu=1.5$nm, $\sigma=0.16$nm</td>
<td></td>
</tr>
<tr>
<td>Pitch (P)</td>
<td>Chi$^2$ distribution</td>
<td>[Zhang 09]</td>
</tr>
<tr>
<td>Density variations</td>
<td>$\mu=4$nm, $\sigma=0.16$nm</td>
<td></td>
</tr>
<tr>
<td>S/D Doping level (Dop)</td>
<td>Gaussian distribution</td>
<td>[Patil 09b]</td>
</tr>
<tr>
<td></td>
<td>$\mu=1%$, $\sigma=0.1%$</td>
<td></td>
</tr>
<tr>
<td>m-CNT probability ($p_m$)</td>
<td>Uniform distribution</td>
<td>[Patil 09b]</td>
</tr>
<tr>
<td></td>
<td>$0%-33%$</td>
<td></td>
</tr>
<tr>
<td>m-CNT removal probability ($p_{mR}$)</td>
<td>Uniform distribution</td>
<td>[Zhang 06]</td>
</tr>
<tr>
<td></td>
<td>$99.99%-100%$</td>
<td>[Patil 09c]</td>
</tr>
<tr>
<td>s-CNT removal probability ($p_{sR}$)</td>
<td>Uniform distribution</td>
<td>[Zhang 06]</td>
</tr>
<tr>
<td></td>
<td>$10%-40%$</td>
<td>[Patil 09c]</td>
</tr>
</tbody>
</table>

Three scenarios:
- No m-CNT removal ($p_{mR}=0\%$, $p_{sR}=0\%$)
- Non-ideal m-CNT elimination ($p_{mR}=99.99\%$, $p_{sR}=10\%-40\%$)
- Ideal m-CNT removal process ($p_{mR}=100\%$, $p_{sR}=0\%$)
Simulation of CNFET manufacturing variability

The number of CNTs per transistor is determined by the pitch distribution. The diameter, doping, and proportions of m-CNTs and s-CNTs are established. The m-CNT removal process is applied.

10,000 samples

- The Stanford CNFET model was used for the $I_{DS}$ characteristic generation of each CNT component.
- Summation of the N components.

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Simulation of CNFET manufacturing variability

I-V characteristics when an ideal m-CNT removal process is used
\((p_m=33\%, \ p_{mR}=100\%, \ p_{sR}=0\%)\)
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CNFET reliability

CNFET failure probability model

$N_{m\text{-CNT}} = 0$  
$N_{s\text{-CNT}} = 0$  
OPEN DEFECT

$N_{m\text{-CNT}} > 0$  
$N_{s\text{-CNT}} > 0$  
FUNCTIONAL

$N_{m\text{-CNT}} > 0$  
SHORT DEFECT

$$p_{\text{short}} = 1 - (1 - (p_m (1 - p_{mR})))^N$$

$$p_{\text{open}} = (p_m p_{mR} + p_s p_{sR})^N$$

$$p_{\text{failure}} = p_{\text{open}} + p_{\text{short}}$$

N is the expected average number of CNTs in the transistor

This model is good for no m-CNT elimination as well as a m-CNT removal process is applied.
CNFET reliability

Three m-CNT removal scenarios

No m-CNT elimination \( (p_{mR}=p_{sR}=0\%) \)

Ideal m-CNT removal \( (p_{mR}=100\%, p_{sR}=0\%) \)

Non-ideal m-CNT removal

- All m-CNTs and some s-CNTs are removed
  - \( p_{mR}=100\% \)
  - \( p_{sR}=10-40\% \)

Small portion of m-CNTs survives
- \( p_{mR}=99.99\% \)
- \( p_{sR}=10-40\% \)

\( p_m=33\% \) (typical CNT growth methods)

\( p_m=10\% \) (enhanced CNT growth methods)

\( p_m=5\% \) (self-sorting techniques)

\( p_m=1\% \) (self-sorting techniques)

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CNFET reliability

No m-CNT removal

Ideal m-CNT removal

Non-ideal m-CNT removal

Non-ideal m-CNT removal

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CNFET reliability

Simulation results (N=7): no m-CNT removal

SHORTS
CNFET reliability

Simulation results (N=7): Ideal m-CNT removal

OPENS

\[ \text{I}_{\text{DS}} (\mu A) \]

\[ \text{V}_{\text{DS}} (V) \]

\[ \text{I}_{\text{DS}} (\mu A) \]

\[ \text{V}_{\text{GS}} (V) \]
CNFET reliability

Simulation results (N=7): Non-ideal m-CNT removal

OPEN AND SHORTS

\[ I_{DS} (\mu A) \]
\[ V_{DS} (V) \]
\[ I_{DS} (\mu A) \]
\[ V_{GS} (V) \]
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CNFET variability

\( \mu = 55.63 \, \mu A \)
\( \sigma = 8.71 \, \mu A \)

\( \mu = 59.75 \, \mu A \)
\( \sigma = 5.69 \, \mu A \)

\( \mu = 60.06 \, \mu A \)
\( \sigma = 5.24 \, \mu A \)

\( \mu = 60.14 \, \mu A \)
\( \sigma = 4.99 \, \mu A \)

\( p_m = 33\% \)
\( p_m = 10\% \)
\( p_m = 5\% \)
\( p_m = 1\% \)

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CNFET variability

$p_m = 33\%$

$\mu = 0.26 \text{ V}$

$\sigma = 0.02 \text{ V}$

$23.08 \%$

$p_m = 10\%$

$\mu = 0.26 \text{ V}$

$\sigma = 0.01 \text{ V}$

$11.54 \%$

$p_m = 5\%$

$\mu = 0.26 \text{ V}$

$\sigma = 0.01 \text{ V}$

$11.54 \%$

$p_m = 1\%$

$\mu = 0.26 \text{ V}$

$\sigma = 0.02 \text{ V}$

$11.54 \%$

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CNFET variability

$I_{ON}/I_{OFF}$

$p_m = 33%$

$\mu = 1.26 \times 10^6$

$\sigma = 0.65 \times 10^6$

154.76 %

$p_m = 10%$

$\mu = 0.92 \times 10^6$

$\sigma = 0.34 \times 10^6$

103.23 %

$p_m = 5%$

$\mu = 0.86 \times 10^6$

$\sigma = 0.28 \times 10^6$

97.67 %

$p_m = 1%$

$\mu = 0.81 \times 10^6$

$\sigma = 0.26 \times 10^6$

96.29 %

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CNFET variability

CNFETs with a mix of semiconducting and metallic CNTs have low ON–OFF ratio

\[
\frac{I_{ON}}{I_{OFF}} = \frac{N_s I_{s, on} + N_m I_m}{N_s I_{s, off} + N_m I_m}
\]

\[
\frac{\mu(I_{ON})}{\mu(I_{OFF})} = \frac{\mu(N_s)\mu(I_{s, on}) + \mu(N_m)\mu(I_m)}{\mu(N_s)(I_{s, off}) + \mu(N_m)\mu(I_m)}
\]

\[
\frac{\mu(N_s)}{\mu(N_m)} = \frac{p_s (1 - p_{sR})}{p_m (1 - p_{mR})}
\]
CNFET variability
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Conclusions

- CNFETs are promising candidates for building highly energy-efficient digital systems. However, inherent CNT imperfections impose significant challenges to building practical CNFET circuits.

- It is important to evaluate the effects of these imperfections on CNFET performance and yield in order to give a realistic view of the challenges that these devices face nowadays.

- We have presented a methodology of CNFET variability and reliability that based on MATLAB script and the Stanford CNFET HSPICE model, it is able to simulate heterogeneous (non-ideal) transistors.

- Furthermore, a CNFET failure model that takes into account opens and shorts and is good for different m-CNT removal scenarios have been derived.
Conclusions

- From the reliability point of view, m-CNTs must be eliminated because they are cause of short. In a 1-tube CNFET the probability of failure is 0.01 with just a $p_m=1\%$. Moreover, it makes bigger in multi-channel CNFETs.

- The CNFET probability of short can be reduced applying m-CNT removal processes. However the use of m-CNT elimination methods together with density variations cause CNT count variations and then the presence of opens.

- If a non-ideal m-CNT removal is used, some s-CNTs are eliminated and a small portion of m-CNTs survives, there is a unique optimum average of CNTs (gate width) for each CNT synthesis method and m-CNT removal process. It is important note that for the best case ($p_m=1\%, \text{ pmR}=99.99\%, \text{ psr}=10\%$) the CNFET failure probability is in order of $10^{-4}$.

- If an ideal m-CNT elimination could be used, between 5 and 20 tubes are required to have $p_f=10^{-10}$ that means a yield of $\sim 100\%$. 
Conclusions

➢ From the variability point of view, $I_{ON}$ and $I_{ON}/I_{OFF}$ parameters of functional transistors are highly affected by count variations, whereas threshold voltage shows a more moderate fluctuation.

➢ Today, great efforts are being made to improve CNFET device processing and to optimize CNFET circuit design techniques. Only in this way, CNT technology can be one of the most viable options for minimum size transistors less than 7nm, which are expected to be produced early 2020.
REFERENCES


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Terascale Reliable Adaptive Memory System
Thanks for your attention
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