



# Migrating to Intel® Architecture

Intelligent Systems Group  
Intel Corporation

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# Intel® Embedded Design Center

WELCOME TO INTEL® EMBEDDED DESIGN CENTER

## From Ideas Into Embedded Products

Processors, software and technologies to help turn your ideas into applications. [Learn more](#)



### DEVELOPERS

Technologies and tools for software and hardware developers

#### Hardware >

- Intel® Xeon® Processors
- Intel® Core™ Processors
- Intel® Atom™ Processors
- Previous Generations

#### Step-by-Step Design Guide >

- Explore
- Evaluate
- Design
- Build

#### Software >

- Boot Loader Technology
- Intel® Embedded Graphics Drivers (IGD)
- Intel® Embedded Media and Graphics Driver (Intel® EMGD)
- Software Stack

#### Migrating to Intel® Architecture >

From:

- ARM\*
- MIPS\*
- PowerPC\*
- SPARC\*

#### Technology >

- Intel® Active Management Technology for Embedded Systems
- Intel® vPro™ Technology
- Packet Processing on Intel® Architecture
- Signal Processing on Intel® Architecture
- Thermal and Power Management
- More >

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#### Design assistance >

Have an Intel representative contact you about your embedded project needs.

Live support

**Not Available**

Chat in English M-F, 24 hours  
Available in Simplified Chinese  
M-F: 9 AM - 5 PM Beijing Time

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# Migration Design Guide



System Stack

## Part one

1. Port the code to the target operating system
2. Execute the code correctly on one Intel® architecture core
3. Optimize the code for performance on one Intel architecture core

## Part two

4. Apply multi-core software design updates
5. Optimize the software design for multi-core Intel architecture

*Steps 4 and 5 are optional*

# Architecture Differences ARM\* vs. Intel® Architecture

Instructions	ARM* and Intel® architecture instructions are very different. For some instructions there is no one to one (ARM to Intel architecture) equivalent. Refer to <a href="#">Intel® 64 and IA-32 Architectures Software Developer Manuals</a>
Alignment	Pointer alignment, e.g. 1 byte aligned on x86, type dependent on ARM, e.g. 4-byte integer must be 4 byte aligned. Structure size and alignment. E.g. a <code>struct</code> with 3 characters on x86 is 3 bytes; it is 4 bytes on ARM. Intel architecture instructions vary in size and therefore do not require alignment.
Vector Oriented Instructions	ARM uses Vector Floating Point (VFP) instructions, Advance SIMD (NEON), DSP Enhanced Instructions. Intel architecture uses Intel® Streaming SIMD Extensions (Intel® SSE).
Signed vs. unsigned <code>char</code>	<code>char</code> is signed on x86 and unsigned on ARM. <code>CHAR_MIN</code> and <code>CHAR_MAX</code> have different values on x86/ARM. gcc compiler can force all <code>char</code> types to be signed: <code>-fsigned-char</code>
Calling Conventions Specified by ABI	Arguments are passed in registers and on the stack for ARM. For Intel architecture, arguments are passed on the stack.
Byte order (Endianness)	ARM is bi-endian; Intel architecture is little-endian
Bit Fields	ARM is bit ordered depending on endian selection. Intel architecture is "normal bit ordered" aka "up bit ordered"

# Architecture Differences PowerPC\* vs. Intel® Architecture

Instructions	PowerPC* and Intel® architecture instructions are very different. For some instructions there is no one to one (PowerPC to Intel architecture) equivalent. Refer to <a href="#">Intel® 64 and IA-32 Architectures Software Developer Manuals</a>
Alignment	PowerPC instructions are all 4 bytes in size and must be aligned on 4 byte boundaries. Intel architecture instructions vary in size and therefore do not require alignment On PowerPC a bool is 4 bytes. On Intel architecture, a bool is 1 byte. Make the code portable by changing the PowerPC boolean data to an unsigned 32-bit integer.
Vector Oriented Instructions	PowerPC uses AltiVec* instructions. Intel architecture uses Intel® Streaming SIMD Extensions (Intel® SSE)
Divide-by-zero	For Integer divide-by-zero, PowerPC simply returns zero. On Intel architecture, executing this operation is fatal.
Calling Conventions Specified by ABI	Arguments are passed in registers for PowerPC. For Intel architecture, arguments are passed on the stack. Intel architecture has fewer registers than PowerPC and therefore local variables may be stored on the stack as well.
Byte order (Endianness)	PowerPC is bi-endian (primarily configured as big-endian), Intel architecture is little-endian
Bit Fields	PowerPC is "down bit ordered". Intel architecture is "normal bit ordered" aka "up bit ordered"

# Traditional BIOS vs. Boot Loader

## BIOS Open Box Designs

(Requires Flexibility)

- Standard OS compatibility
- Feature richness
- Open to many use cases
- Multiple boot paths
- Extra services and support



## Boot Loader Closed Box Designs

(Static Hardware Configurations)

- Custom OS & applications
- Basic Intel® architecture initialization
- Quick and small
- Single use case
- Limited boot options
- No frills
- Royalty free
- No hand-holding



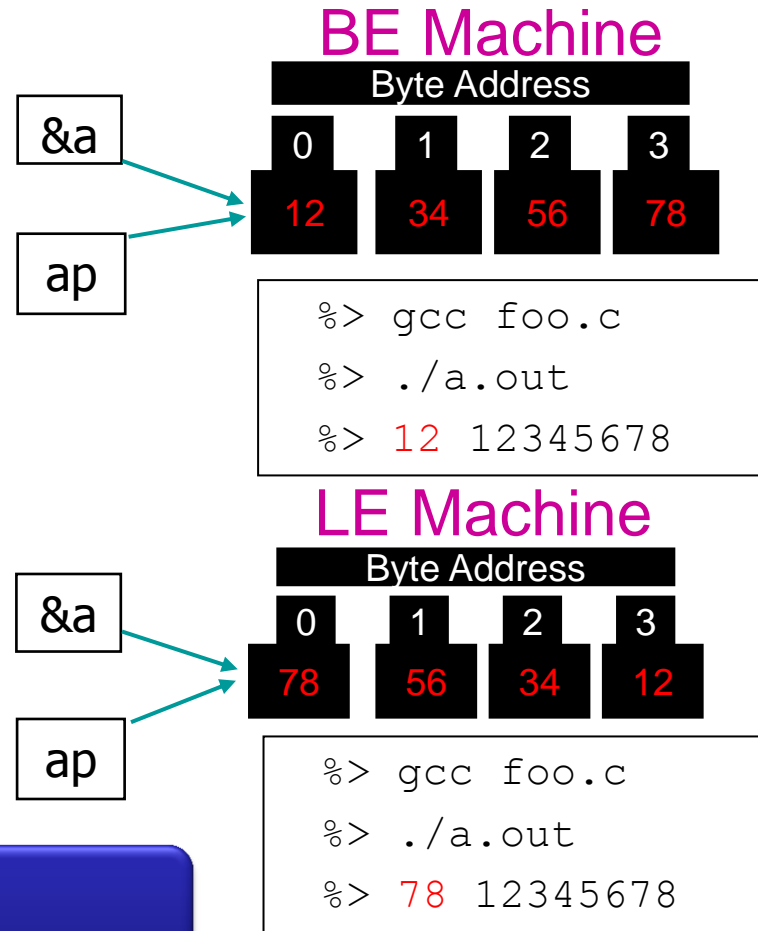
# Endianness and Execution Difference

## Example foo.c

```
#include <stdio.h>
int a = 0x12345678;
int main()
{
    char *ap = (char *) &a;
    printf("%2x %x\n", *ap, a);
    return 0;
}
```

*Different results on  
BE and LE machines!*

*Endian neutral code is portable*





# Software Development Tools

# Intel® Software Development Products



Windows\*

Intel® C++ Compiler for Windows\*  
 Intel® Integrated Performance Primitives (Intel® IPP) Library  
 Intel® VTune™ Performance Analyzer  
 Intel® Parallel Studio  
 Intel® Threading Building Blocks



Moblin\*/Linux\*

Intel® Embedded Software Development Tool Suite  
 Intel® Application Software Development Tool Suite

RTOS

Intel® C++ Compiler Professional Edition for QNX\*  
 Neutrino\* RTOS

## "Application Suite"

- For ISVs and Moblin Community – tune Moblin\* applications for more performance and extend battery life of Intel® Atom™ processor powered devices

<http://software.intel.com/en-us/articles/intel-application-tool-suite-documentation/?wapkw=atom+application+development+tool+suite>

## "Embedded Suite"

- For OEM/ODMs (+ their key ISVs) and OSVs – use a complete tools solution with a sophisticated JTAG debug solution for embedded system and application software design

<http://software.intel.com/en-us/articles/intel-tools-for-intel-atom-processors/>



# Intel® Integrated Performance Primitives (Intel® IPP) Library

Highly optimized multimedia functions

- Images & video
- Communication & signal processing
- Data processing

Fully utilizing

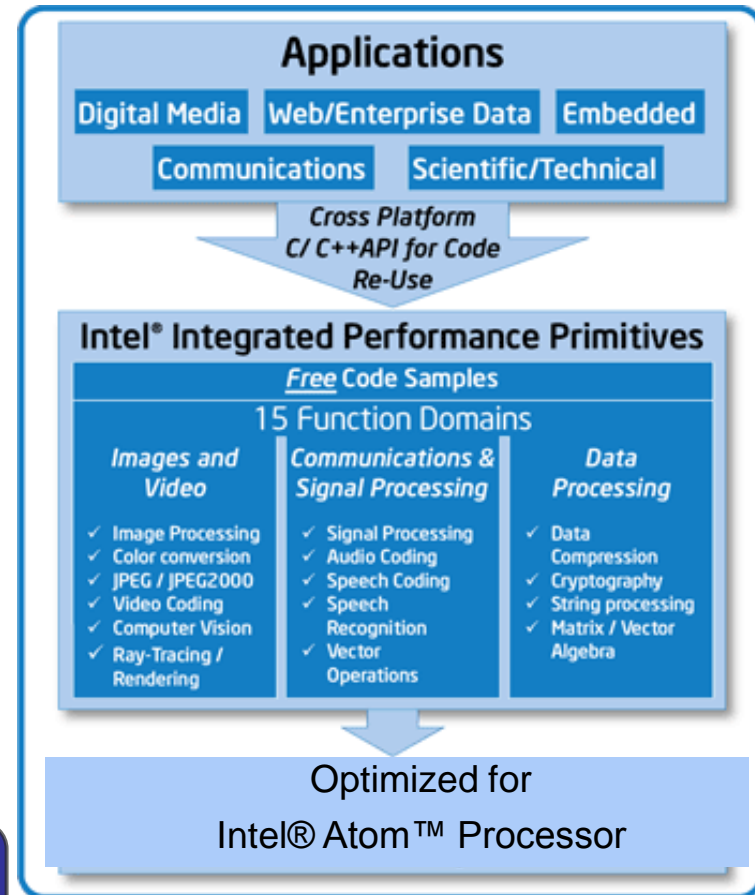
- Intel® Wireless MMX™ technology
- Intel® Streaming SIMD Extensions 2,  
Intel® Streaming SIMD Extensions 3
- Multi-core / HT technology

Rapid application development

Cross-platform compatibility & code re-use

Outstanding performance

*Use Intel® Integrated Performance Primitives libraries to concentrate on new features rather than optimizing application performance*



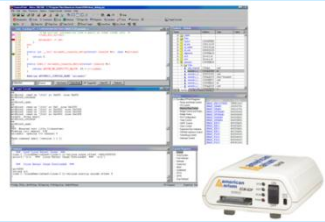
# Architecture Migration Tools

# HW Assisted Development environments

## JTAG support for embedded Intel® processors



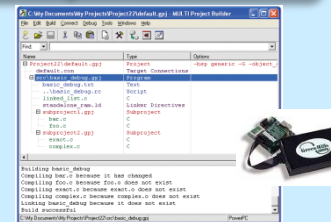
### Arium\* SourcePoint\*



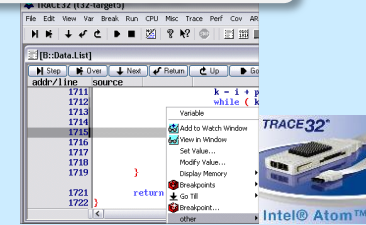
### Wind River\* Workbench\*



### Green Hills\* Software Inc.



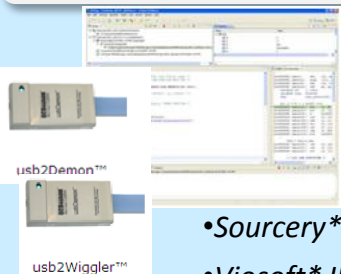
### Lauterbach\* Trace 32\*



## JTAG support for Intel® Atom processor

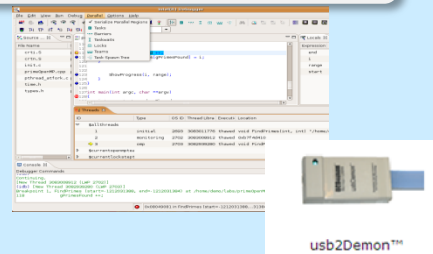


### Macraigor Systems\* OCDemon\*

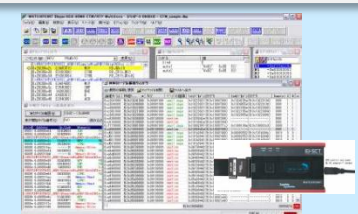


- Sourcery\* CodeBench\*
- Viosoft\* IDE

### Intel® Embedded Software Development Tool Suite



### Sofia Systems\* WatchPoint\*



\*Only Intel® Atom™ processor E660, IJKK

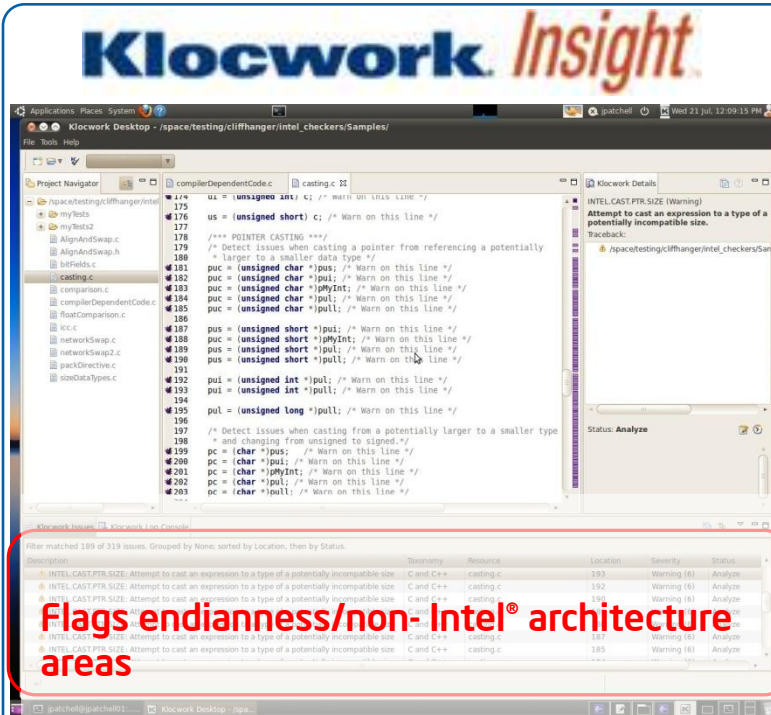


# AltiVec\* to Intel® Streaming SIMD Extensions translation

- N.A. Software\* Vector Oriented Code Conversion Tools bring three tools to market for Linux\* and Wind River\* VxWorks\* operating systems, which will reduce the Digital Signal Processing (DSP) software conversion effort
  - *Vector Signal Image Processing Library (VSIPL)*
  - *AltiVec.h include file for Intel® architecture*
  - *AltiVec\* assembler to Intel® compiler assembler*
- Downloads available from Intel® Embedded Design Center (Intel® EDC)
  - N.A. Software Conversion Tool download ([AltiVec SIMD Macros Translator](#))
  - [N.A. Software Conversion Tools](#)
  - [AltiVec/SSE Migration Guide](#)
  - [Tools For Moving AltiVec DSP Applications to Intel® Processors - Presentation](#)
  - [Tools for Moving AltiVec DSP Application to Intel Processors – Audio Enable Presentation](#)



# Static Code Analysis Tool with Porting and Endian Checkers



## Static code analysis tool for code development

- Includes productivity tool for porting and endianness analysis for migrating to Intel® architecture

## Porting analysis driven checkers:

- For example: warn on tx/rx, arrays, Endian Vulnerability, Concurrency Analysis, casting, bit-field, assembly

**AVAILABLE NOW!**

Available in Klocwork Insight\* 9.2 and Insight Pro 2.2

## New C/C++ Multicore, multiprocessor design checkers:

[http://www.klocwork.com/products/documentation/current/What's\\_New#New\\_C.2FC.2B.2B\\_checkers](http://www.klocwork.com/products/documentation/current/What's_New#New_C.2FC.2B.2B_checkers)

## Multicore and Endianenss White Paper:

<http://www.klocwork.com/resources/endian-deadlock-multicorechallenges>

# References

Intel® Embedded Design Center <http://edc.intel.com/>

**Intel Press book: "Break Away with Intel® Atom™ Processors"**

[http://www.intel.com/intelpress/sum\\_ms2a.htm](http://www.intel.com/intelpress/sum_ms2a.htm)

Intel® 64 and IA-32 Architectures Software Developer's Manuals

<http://developer.intel.com/products/processor/manuals/>

Intel® Software Network <http://software.intel.com>

Intel Tools for Intel Atom Processors

<http://software.intel.com/en-us/articles/intel-tools-for-intel-atom-processors/>

N.A. Software\* Conversion tools

<http://www.nasoftware.co.uk/home/index.php/products/conversion-tools>

Klocwork Insight\* code productivity tools

<http://www.klocwork.com/products/insight/>



*Questions?*